REMARKS

Claims 1-12 are pending in the application. Applicants amended claims 1 and 8 to clarify the invention. Applicants refer to Fig. 3 and its corresponding description in the specification for an exemplary embodiment and support for the claim amendments. No new matter has been added.

Claims 1-2 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,145,686 to McMurray et al. in view of U.S. Patent No. 5,076,133 to Toda; and claims 8-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McMurray et al. in view of Toda, and further in view of U.S. Patent No. 5,732,233 to Klim et al. Applicants amended claims 1 and 8 in a good faith effort to further clarify the invention as distinguished from the cited prior art references. The Examiner's claim rejections are respectfully traversed.

The Examiner relied upon the description of a "memory 28" and a "sequencer 41" in McMurray et al. as disclosure of the claimed features of the "packet data access part" and the "processor," respectively. Applicants respectfully submit that the cited portions of McMurray et al. fail to disclose the claimed features.

The "sequencer 41" (applied to the claimed "processor") only receives data from the "memory 28" (applied to the claimed "packet data access part") through "channel 52" and "channel 30," as shown in Figs. 2-4 and their corresponding description in McMurray et al. The "channel 52" includes a "channel 118," which is a relay of "channel 25" from "data lift 22," and a "channel 119," which is an output from the first "shift register 100" in the "memory 28." And the "channel 30" is the output from the last "shift register 104" in the "memory 28." Finally, an output from the last "shift register 104" in the "memory 28" provides a pulse "line 235" to a

"controller 172" in the "sequencer 41." The only signal from the "sequencer 41" to the "memory 28" is a pulse "line 56" for providing a clocking signal to the shift registers.

As such, the cited portions of McMurray et al. do not disclose,

> "the processor and the packet data access part are directly connected by a read data line and a write data line; the processor reads out or writes data from or to the packet data access part by synchronizing the cycle time of the processor by the read data line and the write data line," as recited in amended claims 1 and 8. (Emphasis added)

Since the Examiner relied upon McMurray et al. to disclose this feature, a combination with the other cited prior art references in the manner proposed by the Examiner would still fail to teach this feature, even assuming such a combination would have been obvious to one skilled in the art.

The Examiner acknowledged that McMurray et al. fail to "teach each of the plurality of registers of the packet data access part is connected to a neighbor register via a selector which selects write data from the processor [or] the neighbor register," page 3, lines 16-18 of the Office Action, and relied upon Toda as a combining reference that allegedly discloses this feature.

Applicants respectfully submit that it would not have been obvious to one skilled in the art to combine Toda with McMurray et al. in the manner proposed by the Examiner. McMurray et al. describe a data compressor that includes a series of shift registers for compressing digital signals to be transferred to a storage device by eliminating redundant signals (please see, e.g., the abstract of McMurray et al.), whereas Toda describes a musical tone signal generator that includes a number of registers for storing waveform information from various stages of modulation operations. Therefore, the two references utilize their respective registers for completely different applications and neither reference provides any suggestion or motivation to be combined with the other. Accordingly, Applicants respectfully submit that it would not have

been obvious to one skilled in the art to combine these references in the manner proposed by the Examiner at the time the claimed invention was made, and that such a combination constitutes improper hindsight from the claimed invention.

Furthermore, although the cited portions of Toda describe connecting a register to a selector, the described selector merely selects between the output of the register (what is already stored in the register) and the output from another connected register in response to a "write signal," which is merely a control signal for the selector. (Please see Fig. 5 and its corresponding description in Toda) In other words, the cited portions of Toda do not add significant functionality beyond the "clock pulse 56" described in McMurray et al. As such, even assuming, arguendo, that it would have been obvious to combine the references, the combination would still fail to teach or suggest,

> "each of the plurality of registers of the packet data access part is connected to a neighbor register via a selector which selects write data from the processor or the neighbor register, so as to enable the processor to process the received packet, instead of fully shifting the received packet through the entire series of registers," as recited in amended claims 1 and 8. (Emphasis added)

With respect to claim 8, the Examiner further acknowledged that the combination of McMurray et al. and Toda would still fail to "teach a plurality of processors being connected in series in that packet sequentially passes through the plurality of processors [instead] of plurality of registers connected in series." Page 6, lines 11-13 of the Office Action. The Examiner, thus, relied upon Klim et al. as a combining reference that allegedly discloses this feature.

As stated above, Applicants submit that it would not have been obvious to one skilled in the art to combine the references in the manner proposed by the Examiner. Additionally, the Examiner relied upon Klim et al. only for allegedly disclosing "a plurality of processors being connected in series." Thus, even assuming, arguendo, that it would have been obvious to

combine the references, the combination would, at most, describe a scheme where processors connected in series, as described in Klim et al., may be used to perform the functions of the registers described in either McMurray et al. or Toda. And a combination of these references would, therefore, still fail to teach or suggest,

> "each of the plurality of registers of the packet data access part is connected to a neighbor register via a selector which selects write data from the processor or the neighbor register, so as to enable the processor to process the received packet, instead of fully shifting the received packet through the entire series of registers," as recited in amended claims 1 and 8. (Emphasis added)

Applicants respectfully submit that amended base claim 1, together with claim 2 dependent therefrom, is patentable over McMurray et al. and Toda, individually and in combination, for at least the foregoing reasons. Applicants further submit that amended base claim 8, together with claims 9-10 dependent therefrom, is patentable over McMurray et al., Toda, and Klim et al., individually and in combination, for at least the foregoing reasons.

Claims 3-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McMurray et al. in view of Toda, and further in view of U.S. Patent No. 6,519,225 to Angle et al.; and claims 11-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McMurray et al. in view of Toda, and further in view of U.S. Patent No. 6,081,538 to Donley.

The additional references, Angle et al. and Donley, were cited specifically to address the additional limitations recited in the rejected dependent claims. Therefore, a combination including these additional references would still fail to teach or suggest the cited features of amended base claims 1 and 8 discussed above, even assuming such a combination would have been obvious to one skilled in the art. Accordingly, Applicants respectfully submit that claims 3-7 and 11-12 are patentable for at least the above-stated reasons.

The above statements on the disclosures in the cited references represent the present opinions of the undersigned attorney. The Examiner is respectfully requested to specifically indicate those portions of the respective reference that provide the basis for a view contrary to any of the above-stated opinions.

Applicants appreciate the Examiner's implicit finding that the additional U.S. patents made of record, but not applied, do not render the claims of the present application unpatentable, whether these references are considered alone or in combination with others.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

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